UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,155	10/30/2001	Eliyahou Harari	SNDK.A06US8	8242

66785 7590 01/03/2012

DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION
505 MONTGOMERY STREET
SUITE 800
SAN FRANCISCO, CA 94111

EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

MAIL DATE	DELIVERY MODE
01/03/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ELIYAHOU HARARI, ROBERT D. NORMAN,
and SANJAY MEHROTRA

Appeal 2009-003212
Application 10/000,155
Technology Center 2800

Before JAMES T. MOORE, *Vice Chief Administrative Patent Judge*,
JOSEPH F. RUGGIERO, SALLY G. LANE, SALLY C. MEDLEY,
MAHSHID D. SAADAT, ALLEN R. MacDONALD, and
ROBERT E. NAPPI, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

I. SUMMARY OF THE DECISION

We affirm the decision of the Examiner rejecting claims 63-103.

II. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 63-103. Claims 1-62 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

Appellants' Invention

Appellants' invention relates to semiconductor electrically erasable programmable read only memories (EEprom) (Spec. 1:5-8). According to Appellants, an array of EEprom cells is organized on a chip into sectors allowing all the cells within each sector to be erased at once (Spec. 2:29-32), or any combination of sectors among the chips to be selected and erased simultaneously (Spec. 2:34 – 3:2). Claim 63, which is illustrative of the claimed invention, reads as follows:

> 63. A defect management engine comprising:
>
> a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;
>
> means for accessing at least one of said plurality of groups of data cells and address cells;
>
> means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and
>
> means for outputting data from said accessed group of data cells when said address match condition is detected.

The Rejection

Claims 63-103 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

The Examiner finds the limitation related to "*address cells* storing data and *addresses*" lacks written descriptive support because the Specification provides for storing addresses of the defective cells as defect pointers.[1] The Examiner specifically states (Ans. 3)[2] that:

> Regarding claim 63, lines 2-4, the recitation of "a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses" lacks support for groups of address cells storing addresses.

Referring to pages 16 and 17 of the Specification, the Examiner finds that the description of sector 401 includes no reference to address cells for storing addresses (Ans. 3). The Examiner finds that the relevant portions of the Specification do not "mention about address cells and storing addresses as claimed, but only about the addresses … stored as defect pointers" and also finds that the defect pointers are not the same as addresses stored in address cells (Ans. 4).

Appellants' Contentions

Appellants respond by stating (App. Br. 17)[3] that:

> [S]upport for "a plurality of groups of first cells ..., said cells in each of said groups of first cells ... storing data" is not

---

[1] The Examiner refers to independent claim 63 reciting "address cells" storing "addresses" whereas Appellants focus their arguments on independent claim 98 where "second cells" store "addresses."

[2] We refer to the second or Supplemental Examiner's Answer mailed Jul. 22, 2008.

[3] We refer to the Appeal Brief filed Mar. 18, 2008.

> questioned. It is on "a plurality of groups of ... second cells, said cells in each of said groups of... second cells ... storing ... addresses" that the Office Action bases its rejection.

Appellants point to Figure 5 of their application and its corresponding description in page 17, lines 6-8 of the Specification and state that the claimed address cells correspond to the defect map 409 where the addresses of the defective cells are stored, which indicates possession by Appellants of the claimed invention when the application was filed (App. Br. 18). Appellants respond to the Examiner's findings that the addresses of the defective cells are stored as defect pointers by stating that such elements are not part of the claim and the preamble clearly identifies the claim as a "defect management engine" (*id.*).

Appellants further contend (*id.*) that the rejection is actually "an objection to the *form* in which the addresses are being stored ("pointers"), a limitation not found in the claims." Appellants argue that the Examiner's rejection appears to require support in the Specification not only for the claims as written, but for a specific embodiment (*id.*). In that regard, Appellants urge that "[t]he claims contain ***no such limiting language*** (such as 'wherein said addresses are not stored as pointers' or other such limiting language) that would restrict them in this way" (*id.*).

Lastly, Appellants state that the present claims are either copied from, or correspond to claims found in U.S. Patent 6,141,267(App. Br. 19).[4] Appellants conclude that the Examiner's rejection improperly requires support for the claims as written as well as for a specific embodiment of

[4] Claim 63 of the instant application is identical to claim 1 of U.S. Patent No. 6,141,267, issued Oct. 31, 2000 (hereinafter "patent '267").

U.S. Patent 6,141,267 and therefore, the correct inquiry is "whether the present specification is enabling for the claim ***as written***" (*id.*).

III. ISSUE

Under 35 U.S.C § 112, first paragraph, with respect to appealed claims 63-103, would the skilled artisan have recognized in Appellants' disclosure a description of the claimed invention in accordance with the "written description" requirement of the statute?

IV. FINDINGS OF FACT

The following findings of fact (FF) are relevant to the issue involved in the appeal.

Appellants' Specification

1. Appellants' Figure 5 is reproduced below:

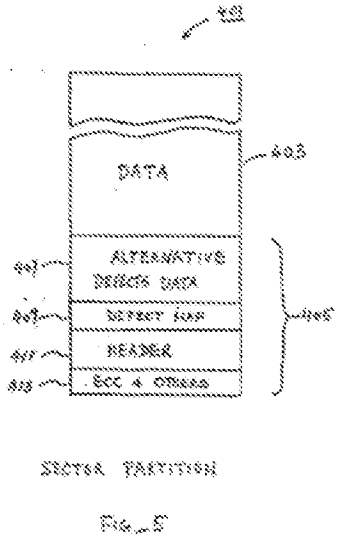

Figure 5 is a schematic illustration showing the partitioning of a Flash EEprom sector into a data area and a spare redundant area (Spec. 5:18-20).

2. Appellants' Specification describes organizing the memory architecture for the cell remapping scheme, as illustrated in Figure 5, into sectors where the cells in each sector are erasable together (Spec. 16:23-26).

3. The organization of the memory architecture is further described as follows:

> The memory architecture has a typical sector 401 organized into a data portion 403 and a spare (or shadow) portion 405. The data portion 403 is memory space available to the user. The spare portion 405 is further organized into an alternative defects data area 407, a defect map area 409, a header area 411 and an ECC [error correction codes] and others area 413.

(Spec. 16:26-32).

4. Appellants describe the error correction operation as follows:

> Whenever a defective cell is detected in the sector, a good cell in the alternative defects data area 407 is assigned to backup the data designated for the defective cell. Thus even if the defective cell stores the data incorrectly, an error-free copy is stored in the backup cell.

(Spec. 17:1-6).

5. Appellants further explain storing the defective cells and the backup cells as follows:

> The addresses of the defective cell and the backup cell are stored as defect pointers in the defect map 409.

(Spec. 17:6-8).

U.S. Patent No. 6,141,267

6. Patent '267 describes a defect management engine (DME) that integrates in the same array a plurality of redundancy data cells used for replacing defective cells and a plurality of redundancy address cells for storing the addresses of the defective cells (Abstract).

7. As shown in Figure 2, the DME 230 uses redundancies included therein for repairing faults (labeled X) found in any domain within anyone of the memories 210. The DME 230 comprises a memory array 232 which includes redundancy data cells 232-0, which are used for replacing defective cells within the memories 210, and redundancy address cells 232-1, which store the addresses to identify the defective cells within the memories 210. (Col. 4, l. 58 – col. 5, l. 7.)

8. Similarly, Figure 8 shows another memory module configuration 800 consisting of a plurality of memory chips 870, each having a memory 810 and DME 830, and a non-volatile random access memory (NVRAM) chip used as a non-volatile redundancy address storage 840 (col. 10, ll. 5-11).

9. NVRAM 840 stores one or more redundancy addresses corresponding to a plurality of addresses of defects in the memory chips 870, which at power-up are copied from NVRAM 840 to the appropriate DME 830 in order to manage the defects in any memory chips 870 (col. 10, ll. 11-23).

V. PRINCIPLES OF LAW

Written Description

"The purpose of the written description requirement is to prevent an applicant from later asserting that he invented that which he did not; the applicant for a patent is therefore required 'to recount his invention in such detail that his future claims can be determined to be encompassed within his original creation.'" *Amgen Inc. v. Hoechst Marion Roussel Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003) (citing *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1561 (Fed. Cir. 1991)).

While there is no requirement that the claimed invention be described in the identical wording that was used in the Specification, there must be sufficient disclosure to show one of skill in this art that the inventor "invented what is claimed." *See Union Oil Co. of California v. Atlantic Richfield Co.*, 208 F.3d 989, 997 (Fed. Cir. 2000).

The written description must be of sufficient detail to show possession of the full scope of the invention. *Pandrol USA LP v. Airboss Railway Products Inc.*, 424 F.3d 1161, 1165 (Fed. Cir. 2005).

Claim Scope

We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the Specification as it would be interpreted by one of ordinary skill in the art. *In re American Academy of Science Tech Center*, 367 F.3d 1359, 1364 (Fed. Cir. 2004).

The PTO gives a disputed claim term its broadest reasonable interpretation during patent prosecution. *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000). The "broadest reasonable interpretation" rule recognizes

that "before a patent is granted the claims are readily amended as part of the examination process." *Burlington Indus. v. Quigg*, 822 F.2d 1581, 1583 (Fed. Cir. 1987). Thus, a patent applicant has the opportunity and responsibility to remove any ambiguity in claim term meaning by amending the application. *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969).

Additionally, the broadest reasonable interpretation rule "serves the public interest by reducing the possibility that claims, finally allowed, will be given broader scope than is justified." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d at 1364 (quoting *In re Yamamoto*, 740 F.2d 1569, 1571-72 (Fed. Cir. 1984)).

"When a party challenges written description support for an interference count or the copied claim in an interference, the originating disclosure provides the meaning of the pertinent claim language." *Agilent Technologies, Inc. v. Affymetrix, Inc.*, 567 F.3d 1366, 1375 (Fed. Cir. 2009).

VI. ANALYSIS

Based on a review of the record, we disagree with Appellants (App. Br. 17-19) that Appellants' description of storing the addresses of the defective cells as defect pointers in the defect map 409 would have been recognized by one of ordinary skill in the art as providing sufficient support for the claimed address cells storing addresses. We find that Appellants' Specification provides a general teaching for substituting the data in a defective cell with error-free data stored in a backup cell in the alternative defects data area 407 (FF 1-4). Additionally, we find that the addresses of the defective cell and the backup cell are stored as *defect pointers* in the *defect map* 409 (FF 5). Therefore, as acknowledged by Appellants (App.

Br. 18), the defect map 409 corresponds to the claimed address cells (second cells in claim 98) which are required to store addresses. But Appellants' Specification does not describe any addresses stored in the defect map 409. Nor does the fact that an error-free copy of the defective data may be accessed using the defect pointers stored in the defect map 409 reasonably convey Appellants' possession of address cells storing addresses.

While storing addresses, in contrast with storing defect pointers, may have been obvious to one of ordinary skill in the art reading the Specification, the Specification itself must reasonably convey the concept of doing so. We find no words in the original written description conveying the claimed storing addresses. Nor have Appellants established that "defect pointers" are intended to mean the same as "addresses" by the Specification. In other words, some type of conversion from defect pointers in the defect map to obtain the cell address takes place before the substitute data is located.

Additionally, in accordance with the precedent set forth in *Agilent*, when Appellants attempted to provoke an interference by copying claims directly from an issued patent, namely, claim 1 of patent '267, the claims must be interpreted in view of the patent '267 Specification before considering whether the claim language is supported by the present application. *See Agilent*, 567 F.3d at 1375. In deciding the question of which specification to consult when construing a claim whose written description is challenged in an interference, the court in *Agilent* examined two prior art cases, *In re Spina*, 975 F.2d 854 (Fed. Cir. 1992) and *Rowe v. Dror*, 112 F.3d 473 (Fed. Cir. 1997). *Agilent*, 567 F.3d at 1374. Because under the facts of *Agilent*, the question was one of written descriptive

support, the court applied what it called the "Spina rule" to interpret the copied claim. According to the "Spina rule" one looks to the originating specification, i.e., the specification of the patent from which the claim is copied, to construe the claim.

In the present case, there is a real question as to the meaning of the terms "address" and "defect pointers" as used in the patent '267 and the present application, respectively. When one looks to the Specification of patent '267, the meaning of the terms "address cells" and "storing addresses" is clearly defined by stored *addresses* to identify the location of the cells within a memory array (FF 6-9). In that regard, Appellants have not provided evidence to establish that patent '267 uses the terms "pointers" to indicate the stored "address." In contrast, Appellants' Specification merely stores "pointers" which are not necessarily the addresses of the defective cells or the backup cells, but variables that contain and point to the location of the addresses.[5]

---

[5] As found in Microsoft® Computer dictionary, 5th Ed., published by Microsoft Press, March 15, 2002, available online through the link http://academic.safaribooksonline.com/0735614954, "pointer" and "address" are defined as:
pointer *n.* In programming and information processing, a variable that contains the memory location (address) of some data rather than the data itself.
address *n.* **1.** A number specifying a location in memory where data is stored. *See also* **absolute address**, **address space**, **physical address**, **virtual address**. **2.** A name or token specifying a particular computer or site on the Internet or other network. **3.** A code used to specify an e-mail destination.

What Appellants really are attempting to do is to argue that the instant claims do not preclude storing addresses as pointers (App. Br. 18) to provide written descriptive support. As such, the claims, *as written*, may cover storing addresses as pointers, but Appellants' Specification provides written descriptive support only for stored defect pointers, which is different in scope than storing the cell addresses. While the ultimate goal of locating the defective cells and backup cells may be achieved using either pointers or addresses, the claims nonetheless require address cells for storing the addresses, which are repeatedly described in the patent '267 Specification as simply "addresses." Therefore, when we look to the patent '267 to interpret the words of the claim, and not to establish written descriptive support, we do not find sufficient support in Appellants' Specification for the claim term as interpreted based on patent '267. *See Spina*, 975 F.2d at 858; and *Cultor Corp. v. A.E. Staley Mfg.*, 224 F.3d 1328, 1332 (Fed. Cir. 2000) ("When a claim is copied from another patent for interference purposes, it must be supported by the specification of the copier.").

In view of the above discussions and considering the presented facts, the arguments made by Appellants, and the findings, we find no error in the Examiner's finding that Appellants' disclosure lacks written descriptive support for the claimed "address cells" storing "addresses." Therefore, the rejection of claims 63-103 under the first paragraph of 35 U.S.C. § 112 is sustained.

VII. CONCLUSION

Based on the findings of fact and the analysis above, we conclude that:

(1) with respect to the 35 U.S.C § 112, first paragraph, the skilled artisan would have not recognized in Appellants' disclosure a description of the claimed invention in accordance with the "written description" requirement of the statute;

(2) Claims 63-103 are not patentable.

VIII. DECISION

The decision of the Examiner rejecting claims 63-103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

msc